IN THE SPECIFICATION

Please amend the first paragraph on page 1, lines 4-5, as shown below.

--The present invention relates to a computer system with ~~localised~~ localized on-chip debug facility.--

Please amend paragraphs 11 and 12 on page 5, lines 24-27 as shown below.

-- FIG. 9 illustrates schematically FIFOs in the ~~synchronisation~~ synchronization unit; and

FIG. 10 illustrates a timing diagram for operation of the ~~synchronisation~~ synchronization unit.--

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Please amend the first full paragraph on page 6, lines 8-~~20~~ 18-30, as shown below.

--Figure 2 is a more detailed schematic of the processor 4 in combination with selected on-chip emulation functional blocks which form part of the on-chip emulator 6. The processor 4 comprises a processor core 18 which is connected to a program memory 20 which holds code to be executed by the core. The core comprises a prefetch/align stage 22, a decode/dispatch stage 24, a microinstruction generator 26 and four parallel execution pipelines AU_0, AU_1, DU_0, and DU_1. The ~~core~~ processor 4 operates in a pipelined manner such that all stages can be active at the same time, on different instructions. The pipeline stages are denoted by horizontal dotted lines in Figure 2. It will readily be understood that each execution pipeline itself AU_0, AU_1, DU_0, and DU_1 constitutes a number of pipeline stages.—

Please amend the first two paragraph on page 7, lines 1-9, as shown below.

--The program memory 20 contains code in the form of ~~128-bit~~ 128-bit long words. Each word contains a plurality of instructions depending on the instruction mode of the processor. In this respect, reference is made to Figure 3.

According to a first instruction mode, a pair of ~~16-bit~~ 16-bit instructions are supplied during each machine cycle to the decoder 24 from the prefetch/align stage buffer 22. ~~this~~ This